AMENDMENTS TO THE CLAIMS

In the Claims:

Kindly amend the claims as follows:

9. (Currently Amended) A printed wiring board comprising:

(a) a dielectric substrate~~,~~ having upper and lower surfaces;

(b) at least one landless filled plated through hole disposed through the substrate from the upper to the lower surface, the through hole having ~~an outside~~ a first diameter~~, formed by the steps of:~~

~~(a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;~~

~~(b) depositing electrically conductive plating having a thickness on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;~~

~~(c) filling said hole with a filler composition;~~

~~(d) etching said subcomposite to partially remove said electrically conductive layer and thereby reducing the electrically conductive plating thickness to a minimum thickness of about 0.2 mil.;~~

~~(e) removing residual amounts of said filler composition on said subcomposite; and~~

~~(f) etching said subcomposite to completely remove said electrically conductive plating;~~;

(c) the through hole further comprising an inner surface extending from the upper to the lower surface, the inner surface plated with a conductive metal plating, the inner surface plating having an upper end aligned with the substrate upper surface and a lower end aligned with the substrate lower surface;

(d) the through hole filled with a filler composition having upper and surfaces, wherein

the filler composition upper surface is aligned with the dielectric substrate upper surface and the through hole inner surface plating upper end, the filler composition upper surface, substrate upper surface and inner surface plating upper end thereby defining a smooth upper subcomposite surface; and

(c) a first circuitry additively plated onto said ~~dielectric substrate~~ upper subcomposite surface and electrically connect~~ing~~ed to said plated through hole, said first circuitry ~~having~~ further comprising circuit lines having a line width approximately equal to or less than the first diameter ~~of said filled plated through hole, wherein the circuitry is formed by the steps of:~~

~~(g) depositing a seed activator on the surface of said subcomposite including said filler composition;~~

~~(h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and~~

~~(i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole.~~

10. (Currently Amended) The ~~A~~ printed wiring board of claim 9 ~~comprising a dielectric substrate, at least one filled plated through hole, formed by the steps of:~~

~~(a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;~~

~~(b) depositing electrically conductive plating on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;~~

~~(c) filling said hole with a filler composition;~~

~~(d) etching said subcomposite to partially remove said electrically conductive layer;~~

~~(e) removing residual amounts of said filler composition on said subcomposite; and~~

~~(f) etching said subcomposite to completely remove said electrically conductive plating; and~~

~~circuitry on said dielectric substrate connecting to said plated through hole, said circuitry having circuit lines,~~ wherein the ~~circuit lines~~ first circuitry further has~~ving~~ an aspect ratio greater than about 0.5, ~~wherein the circuitry is formed by the steps of:~~

Cancelled D1

~~(g) depositing a seed activator on the surface of said subcomposite including said filler composition;~~

~~(h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and~~

~~(i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole.~~

11. (Currently Amended) The ~~A~~ printed wiring board of claim 10 ~~comprising a dielectric substrate, at least one filled plated through hole, and circuitry on said dielectric substrate connecting to said plated through hole, said circuitry having an~~ wherein the aspect ratio is greater than about 1.

12. (Currently Amended) The invention as defined in claim 9 wherein said first circuitry further comprises ~~includes a~~ an upper conductive metal pad plated onto the through hole inner surface plating upper end and the fill composition upper surface, the pad having a second

diameter about equal to the first diameteron each of said filled plated through holes, wherein each pad diameter is about equal the filled plated through hole diameter.

13. (Currently Amended) The invention as defined in claim 10 wherein said first circuitry further comprises includes a an upper conductive metal pad plated onto the through hole inner surface plating upper end and the fill composition upper surface, the pad having a second diameter about equal to the first diameteron each of said filled plated through holes.

Cont'd D1

14. (Currently Amended) The invention as defined in claim 11 wherein said first circuitry further comprises includes a an upper conductive metal pad plated onto the through hole inner surface plating upper end and the fill composition upper surface, the pad having a second diameter about equal to the first diameteron each of said filled plated through holes.

15. (Currently Amended) The invention as defined in claim 9 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

16. (Currently Amended) The invention as defined in claim 10 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

17. (Currently Amended) The invention as defined in claim 11 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry on

said dielectric substrate, said layer of dielectric material having at least one via formed therein.

18. (Currently Amended) The invention as defined in claim 15 further characterized by a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry through the at least one via.

19. (Currently Amended) The invention as defined in claim 16 further characterized by a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry through the at least one via.

Cont'd D1

20. (Currently Amended) The invention as defined in claim 17 further characterized by a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry through the at least one via.

21. (Cancelled)

22. (New) The invention as described in claim 9, wherein the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates.

23. (New) The invention as described in claim 10, wherein the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates.

D2

24. (New) The invention as described in claim 11, wherein the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates.

25. (New) The invention as described in claim 9, wherein the inner surface conductive metal plating has a thickness, the thickness from about 0.1 mils to about 4.0 mils.

Cont'd D2

26. (New) The invention as described in claim 10, wherein the inner surface conductive metal plating has a thickness, the thickness from about 0.1 mils to about 4.0 mils.

27. (New) The invention as described in claim 11, wherein the inner surface conductive metal plating has a thickness, the thickness from about 0.1 mils to about 4.0 mils.